REMARKS

Claims 1-3 and 6-13 are pending in the present application. Claims 1-14 were rejected in the Office Action mailed October 12, 2005. Claims 4, 5 and 14 are canceled herein without prejudice. Claims 1, 7, 8, 11 and 12 are amended herein. No new matter is presented as a result of these claim amendments. The Examiner's rejections are traversed below. Applicants respectfully request the Examiner to consider and allow the remaining claims.

Claim Rejections – 35 USC § 102

Claims 8 and 14

Claims 8 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Karp et al. (U.S. Patent No. 6,266,269 B1; hereinafter "Karp"). Claim 14 is canceled herein without prejudice.

Claim 8 recites:

> An integrated circuit device comprising a first non-volatile **flash** memory cell comprising:
> a first **stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer**; and
> a first region under said first stacked gate structure comprising overlapping lateral diffusions of source and drain implantation regions.
> *(emphasis added)*

Karp teaches a programmed storage transistor **200** (Figure 2C) in a memory cell **301** (Figure 3A) formed "using standard CMOS processes" (col. 5, line 2), as opposed to the flash memory cell recited in Claim 8. Karp teaches that memory cell **301** "includes a write access transistor **302**, a storage transistor **303**, and a read access

transistor **304**" (col. 6, lines 27-29). Karp teaches that storage transistor **303** is a "low voltage NMOS device" (col. 6, line 36). An NMOS device employed as a storage transistor in a memory cell described by Karp is not a flash memory cell as recited in Claim 8. As can be appreciated by one skilled in the art, a flash memory cell is a modified NMOS transistor with an additional conductor suspended between the gate and the source/drain terminals.

Furthermore, the process by which Karp's source **202A** and drain **202B** diffuse laterally and merge, as illustrated in Figure 2C, also fuses the layers of the gate structure (**201** and **203** in Figure 2A) to form the fused structure **204** in Figure 2C. In contrast, flash memory cell recited in Claim 8 has overlapping source and drain regions *and* a stacked gate structure having separate control gate, charge trapping layer and insulating layers.

Applicants respectfully submit that the integrated circuit device recited in Claim 8 is not anticipated by Karp, and that the rejection of Claim 8 under 35 U.S.C. 102(b) is traversed. Applicants respectfully request allowance of Claim 8.

Claim Rejections – 35 USC § 103

Claims 1-7

Claims 1 thru 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. (U.S. Patent No. 6,765,257 B1; hereinafter "Mehrad") in view of Karp. Claims 4 and 5 are canceled herein without prejudice.

Claim 1 recites:

An integrated circuit device comprising:

an array of **flash** memory cells, said cells comprising a source, a drain and **a stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer**, wherein a region under said stacked gate structure comprises overlapping lateral diffusions of implantation regions of said source and said drain;

a common source line coupled with said source; and

a source contact disposed outside of said common source line and coupled with said source, wherein said source contact is coupled to said common source line under said stacked gate structure, and wherein said source contact is disposed in a row with drain contacts. *(emphasis added)*

Mehrad teaches a flash memory array, but Mehrad fails to teach or suggest a region under a stacked gate structure having overlapping lateral diffusions of source and drain regions, as recited in Claim 1. Karp teaches an NMOS device that is a storage transistor **200** for a memory cell **301**, having overlapping source and drain regions and fused gate structures **204** as shown in Karp's Figure 2C. As can be appreciated by one skilled in the art, and as taught by Mehrad, flash memory cells require a floating gate **13** and a control gate **14** (Mehrad, col. 1, line 22). It would be undesirable for a cell in Mehrad's array to have the fused structure **204** depicted in Karp's Figure 2C. There is no motivation to combine the NMOS device **200** taught by Karp with the flash memory array taught by Mehrad.

Applicants respectfully submit that Claim 1 and Claims 2, 3, 6 and 7 dependent on Claim 1 are patentable over Mehrad in view of Karp, and the rejection of Claims 1, 2, 3, 6 and 7 under 35 U.S.C. 103(a) is traversed. Applicants respectfully re quest allowance of Claims 1, 2, 3, 6 and 7.

Claims 9-13

Claims 9 thru 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp as applied to Claims 8 and 14 and further in view of Mehrad. Claims 9-13 are dependent on Claim 8. Claim 8 is believed to be allowable for the reasons discussed above.

Mehrad does not remedy the deficiencies in Karp with regards to Claim 8. Specifically, Karp teaches an NMOS device that is a storage transistor **200** having overlapping source and drain regions and a fused structure **204** where a stacked gate structure used to be. Mehrad teaches a flash memory array, but fails to teach overlapping source and drain regions. Therefore, the combination of Mehrad with Karp does not produce the flash memory array having overlapping source and drain regions and stacked gate structures as recited in Claims 9-13, dependent on Claim 8. There is no motivation to apply the teachings of Mehrad to the teachings of Karp, as Karp does not teach a flash memory array.

Applicants respectfully submit that Claims 9-13 are patentable over Karp in view of Mehrad, and that the rejection of Claims 9-13 under 35 U.S.C. 103(a) is traversed. Applicants respectfully request allowance of Claims 9-13.

CONCLUSION

In light of the response presented herein, Applicants respectfully assert that Claims 1-3 and 6-13 of the present application overcome the rejections of record, and therefore earnestly solicit allowance of these claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
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